CLAIMS:

1. A host coupled to a switched fabric including one or more fabric-attached I/O controllers, comprising:

a processor;

a host memory coupled to said processor; and

a host-fabric adapter coupled to said processor and provided to interface with said switched fabric, which caches selected translation and protection table (TPT) entries from said host memory for a data transaction, and flushes individual cached translation and protection table (TPT) entry in accordance with a translation cacheable flag.

2. The host as claimed in claim 1, wherein said host-fabric adapter comprises an internal cache for storing said selected translation and protection table (TPT) entries from said host memory.

3. The host as claimed in claim 2, wherein each of said selected translation and protection table (TPT) entries represents translation of a single page of said host memory.

4. The host as claimed in claim 2, wherein said host-fabric adapter is provided to perform virtual to physical address translations and validate access to said host memory using said

selected translation and protection table (TPT) entries.

5. The host as claimed in claim 2, wherein each of said translation and protection table (TPT) entries comprises:

protection attributes which control read and write access to a given memory region of said host memory;

said translation cacheable flag which specifies whether said host-fabric adapter may flush a corresponding translation and protection table (TPT) entry stored in said internal cache;

a physical page address field which addresses a physical page frame of data entry; and

a memory protection tag which specifies whether said host-fabric adapter has permission to access said host memory.

6. The host as claimed in claim 5, wherein said protection attributes comprise a Memory Write Enable flag which indicates whether said host-fabric adapter can write to page; a RDMA Read Enable flag which indicates whether the page can be source of RDMA Read operation; a RDMA Write Enable flag which indicates whether the page can be target of RDMA Write operation.

7. The host as claimed in claim 5, wherein said host-fabric adapter flushes a designated cached translation and protection table (TPT) entry from said internal cache when said

translation cacheable flag of said designated cached translation and protection table (TPT) entry indicates a first logic state, and maintains said designated cached translation and protection table (TPT) entry in said internal cache when said translation cacheable flag of said designated cached translation and protection table (TPT) entry indicates a second logic state opposite of said first logic state.

8. The host as claimed in claim 1, further comprising an operating system including driver software which sets status of said translation cacheable flag per translation and protection table (TPT) entry for enabling said host-fabric adapter to flush individual cached translation and protection table (TPT) entry from said internal cache.

9. A network, comprising:

a switched fabric;

I/O controllers attached to said switched fabric; and

a host comprising an operating system, a host memory, and a host-fabric adapter which caches selected translation and protection table (TPT) entries from said host memory, and which flushes individual cached translation and protection table (TPT) entry in accordance with a translation cacheable flag.

10. The network as claimed in claim 9, wherein said host-fabric adapter comprises an

internal cache for storing said selected translation and protection table (TPT) entries from said host memory.

11. The network as claimed in claim 9, wherein each of said selected translation and protection table (TPT) entries represents translation of a single page of said host memory.

12. The network as claimed in claim 9, wherein said host-fabric adapter is provided to perform virtual to physical address translations and validate access to said host memory using said selected translation and protection table (TPT) entries.

13. The network as claimed in claim 10, wherein each of said translation and protection table (TPT) entries comprises:

protection attributes which control read and write access to a given memory region of said host memory;

said translation cacheable flag which specifies whether said host-fabric adapter may flush a corresponding translation and protection table (TPT) entry stored in said internal cache;

a physical page address field which addresses a physical page frame of data entry; and

a memory protection tag which specifies whether said host-fabric adapter has permission to access said host memory.

14. The network as claimed in claim 13, wherein said protection attributes comprise a Memory Write Enable flag which indicates whether said host-fabric adapter can write to page; a RDMA Read Enable flag which indicates whether the page can be source of RDMA Read operation; a RDMA Write Enable flag which indicates whether the page can be target of RDMA Write operation.

15. The network as claimed in claim 10, wherein said host-fabric adapter flushes a designated cached translation and protection table (TPT) entry from said internal cache when said translation cacheable flag of said designated cached translation and protection table (TPT) entry indicates a first logic state, and maintains said designated cached translation and protection table (TPT) entry in said internal cache for future re-use when said translation cacheable flag of said designated cached translation and protection table (TPT) entry indicates a second logic state opposite of said first logic state.

16 An apparatus which stores translation and protection table (TPT) entries for virtual to physical address translations, and which flushes individual translation and protection table (TPT) entry stored in accordance with a corresponding translation cacheable flag.

17. The apparatus as claimed in claim 16, further comprising an internal cache for storing said translation and protection table (TPT) entries.

18. The apparatus as claimed in claim 16, wherein each of said translation and protection table (TPT) entries represents translation of a single page of a host memory.

19. The apparatus as claimed in claim 17, wherein each of said translation and protection table (TPT) entries comprises:

protection attributes which control read and write access to a given memory region of a host memory;

said translation cacheable flag which specifies whether said apparatus may flush a corresponding translation and protection table (TPT) entry stored in said internal cache;

a physical page address field which addresses a physical page frame of data entry; and

a memory protection tag which specifies whether said apparatus has permission to access said host memory.

20. The apparatus as claimed in claim 19, wherein said protection attributes comprise a Memory Write Enable flag which indicates whether said apparatus can write to page; a RDMA Read Enable flag which indicates whether the page can be source of RDMA Read operation; a RDMA Write Enable flag which indicates whether the page can be target of RDMA Write operation.

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